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He introduced the NoC in ST and he is responsible of Spidergon STNoC program; managing architecture, design, prototyping and modeling teams. Moreover, he is coordinating several world-wide university and European research programs. His research interests include design methodologies for system-on-chip, with particular emphasis to network-on-chip, multicore and many-core architectures, parallel programming and system level design. He has published several research articles in various books and journals. He was a member of the OSCI language working group contributing towards SystemC2.0 definition and OSCI standardization. He was an early introduced of SystemC in ST. He has been chair of many international conferences on SoC design and has helped in organizing several others. He has been a program committee member of DATE, FDL, CODES+ISSS and DAC and has contributed to the MEDEA+ EDA and CATRENE EDA Roadmaps. He is joint inventor on 18 international patents and he is member of the EDAA (European Design Automation Association)